Release 2022 R1 Highlights Photonics (Lumerical)



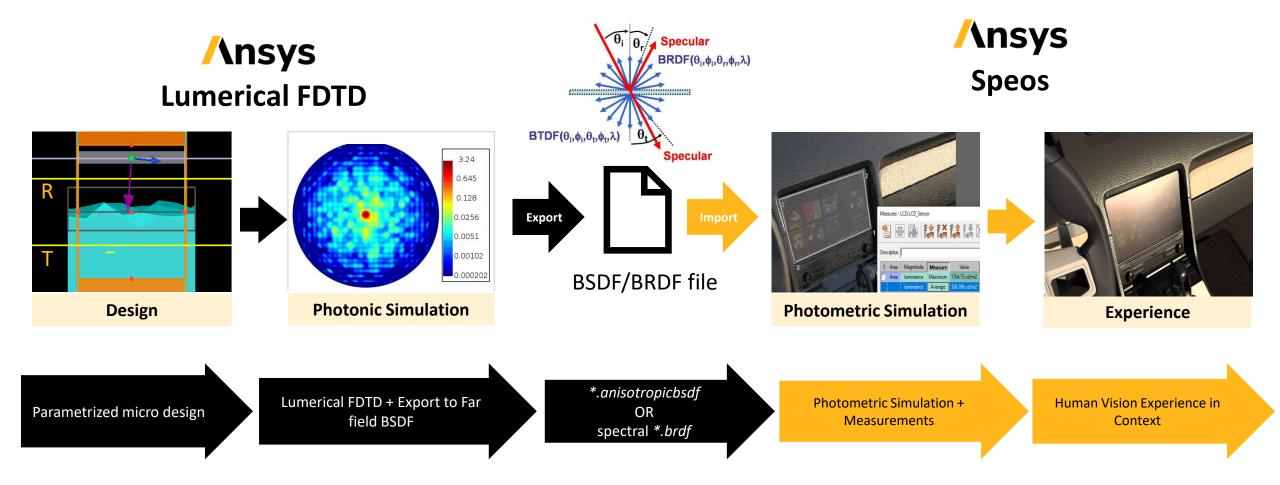
Ansys Cloud HPC Services Integration

- Native UI widget in-product for interfacing with Ansys Cloud HPC Services
 - login, connection status, job submission/monitoring/ control, file upload/download
- Support for Batch (distributed) Solves and Parametric Sweeps
- Complements the VDI access to Ansys Cloud Direct introduced in 2021 R2

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Name	State	Start time	Finish time	Progress	Download state		ld
y of CppStartedJob	Running	07/07/2021 11:48:27 AM		New Job			×
olver: PN_phase_shifter	Running	18/11/2021 7:02:08 PM		Hardware settings			
olver: voltage_1	Running	19/11/2021 3:06:07 PM		Region	eastus		~
olver: voltage_1	Completed	22/11/2021 2:22:32 PM	22/11/2021 2:26:49 PM	Machine type	HB60rs		~
olver: voltage_2	Completed	22/11/2021 2:22:54 PM	22/11/2021 2:27:16 PM	Total number of cores			60 🜩
olver: voltage_3	Completed	22/11/2021 2:23:17 PM	22/11/2021 2:28:20 PM	Solver Settings			
olver: voltage_e_1	Queued	23/11/2021 11:45:02 AM		Version 2021R2			
olver: voltage_e_2	Stopped	23/11/2021 11:45:25 AM	23/11/2021 11:49:05 AM	Active solver FDE			
olver: voltage_e_3	Stopped	23/11/2021 11:45:49 AM	23/11/2021 11:48:35 AM	Show advanced o	puons		
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SPEOS Surface Models: BSDF/BRDF Format Exchange (BETA)



Applications: Diffusive films for displays, scattering from micro-textured surfaces, human skin models,...

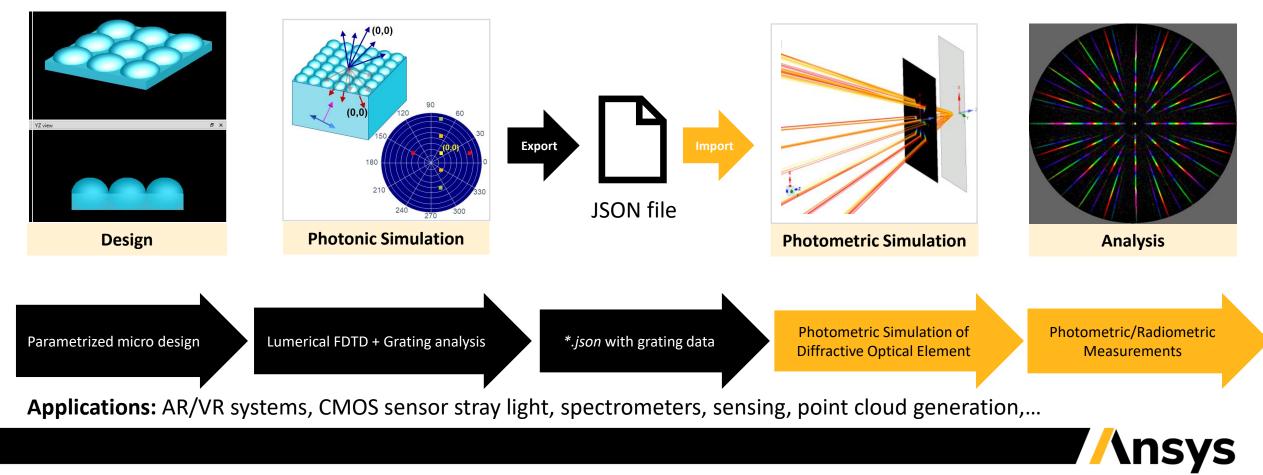
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SPEOS surface models: Diffraction Grating SOP Plugin (BETA)

Ansys Lumerical FDTD

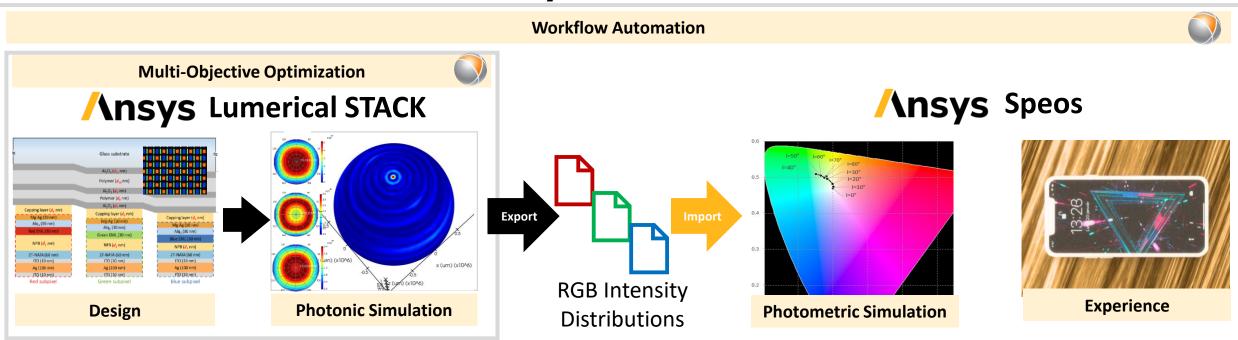
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Display optimization workflow and enhancements in optiSLang integration (BETA)

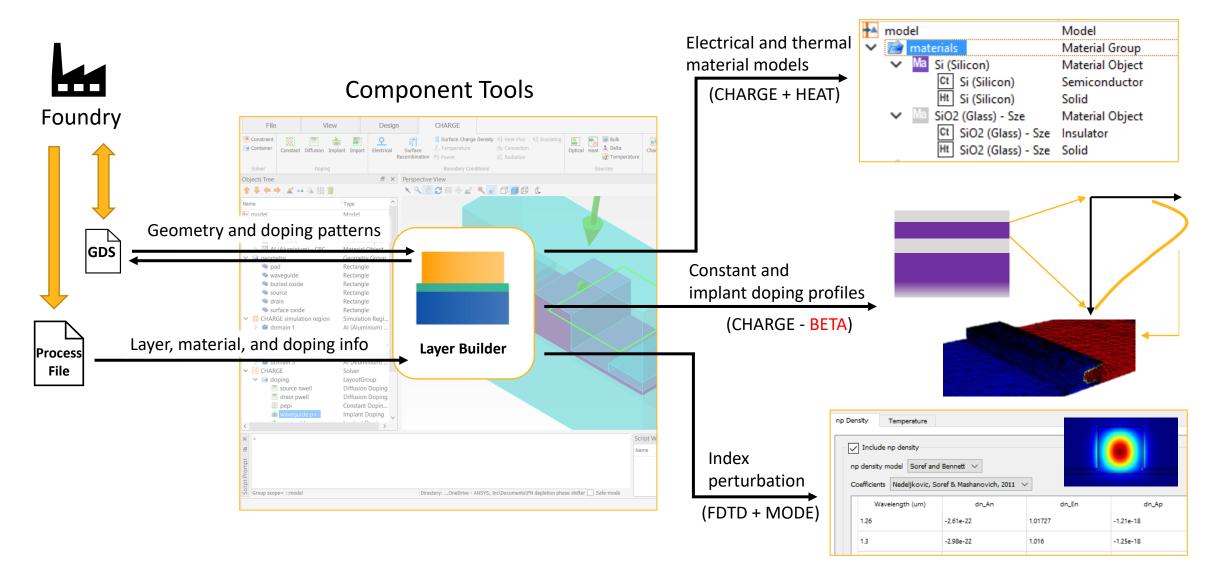




Fully leverage fast STACK simulations in optiSLang workflow with enhanced integration:

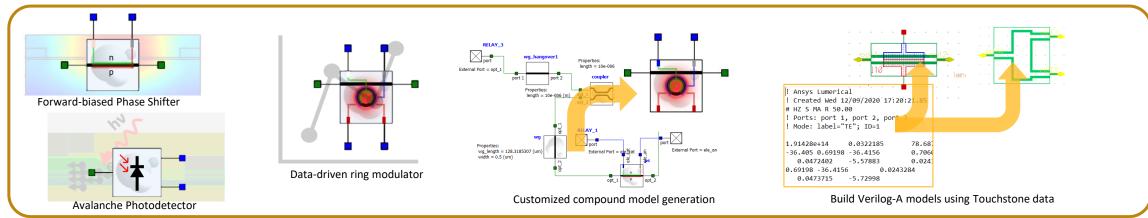
- Lumerical application persists throughout iterations, avoiding additional start-up overhead
- Lumerical script files can be run directly without loading or running a project file

Process Enabled Active Photonic Component Design (BETA)



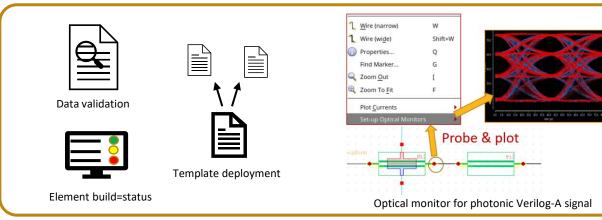


CML Compiler & Verilog-A Feature Updates

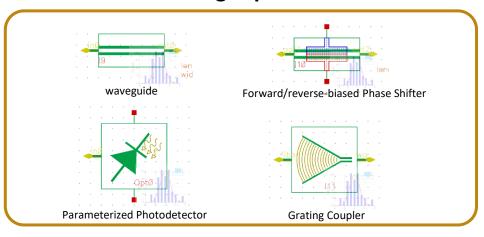


New and improved INTERCONNECT and Verilog-A photonic models

Improved usability



Statistical Verilog-A photonic models





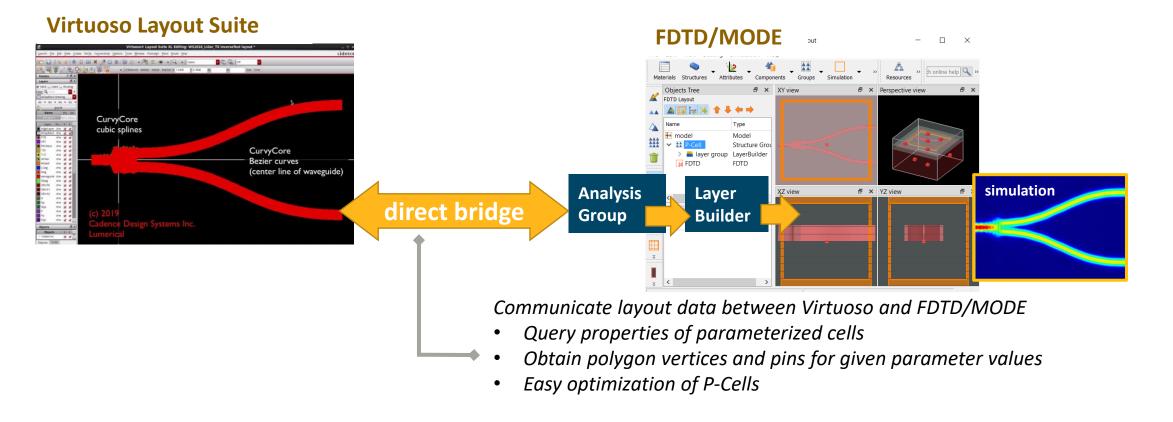
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Virtuoso Layout Integration

Design Challenges:

- Users need to define layouts in both layout editor and FDTD/MODE solvers, which is time-consuming
- Inconsistency between two layouts is difficult to resolve
- Exporting GDS to FDTD/MODE does not support parametric analysis

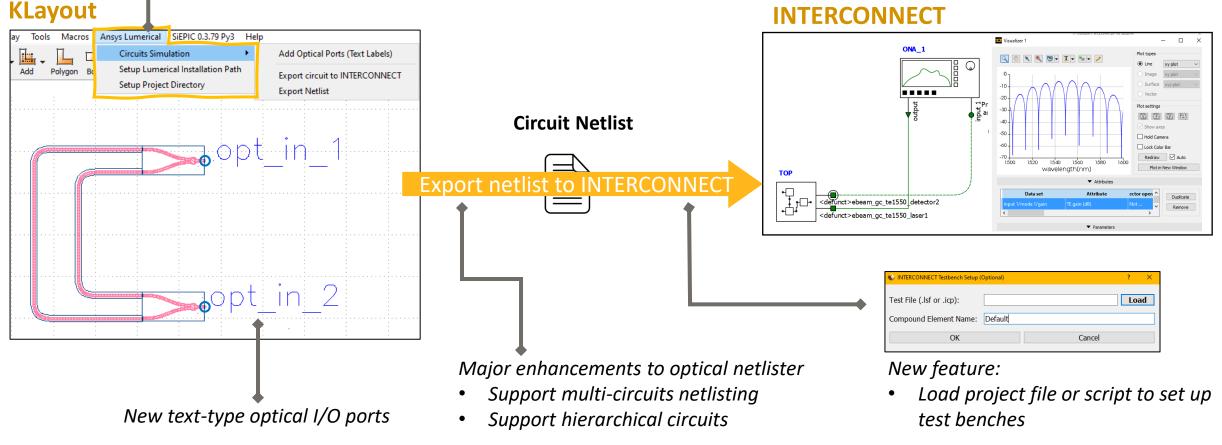
Goal: Facilitate component design through direct integration with Virtuoso Layout



KLayout Integration

Ansys-Lumerical Package

- Open-source project in collaboration with SiEPIC program
- **Goal**: create integration to support photonic layout-driven circuit designs and simulations

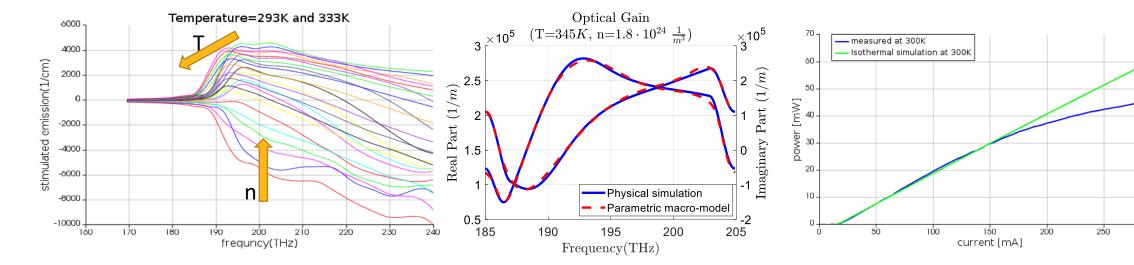


INTERCONNECT

Insys



 Self-heating limits the output power and efficiency of the laser, impacts adjacent devices



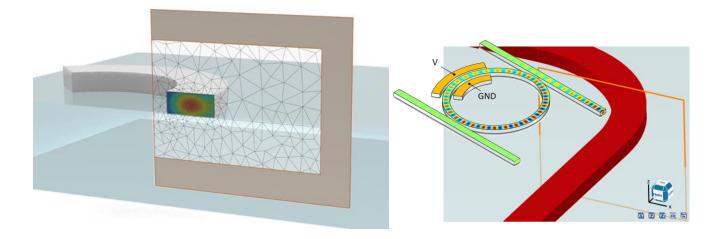
Material gain from physical simulation or measurement: parameterized by carrier density & temperature Reduced order model accurately fits & interpolates *arbitrary* gain spectra Fast simulation of steady state laser power vs. current with physics-informed accuracy



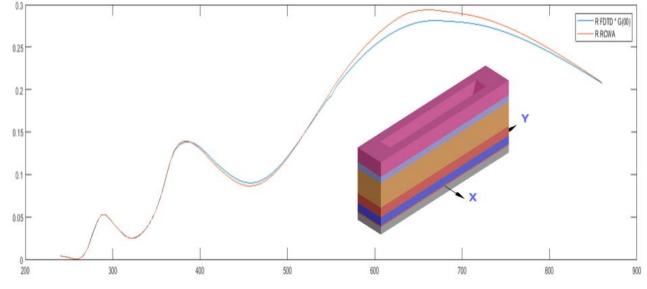
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Photonics Core Technologies

• New waveguide bend calculation in FEEM for bend loss and ring analysis



- Calculate diffracted order efficiencies of 1D and 2D gratings with new of RCWA solver (BETA)
 - Script interface available in FDTD
 - Dielectric materials, periodic boundaries



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